

Appl. No. 10/714,285

Response dated July 29, 2005

Reply to Office action dated Jun. 29, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

1. (currently amended) A ~~recessed-bond~~ semiconductor package substrate comprising:
a first metal layer adapted to receive a semiconductor die;
an underlying metal layer configured for direct interconnections to the semiconductor die;
and
a dielectric layer between the first metal layer and the underlying metal layer, including a region of opening to uncover a portion of the underlying metal layer for the direct interconnection to the semiconductor die, wherein the underlying metal layer is configured for a direct interconnection, through the first metal layer and the dielectric layer, with a semiconductor die.
2. (original) The semiconductor package substrate of claim 1, wherein the direct interconnection is formed by at least one bond wire.
3. (currently amended) The semiconductor package substrate of claim ~~[[1]]~~ 2, wherein ~~at least one the opening region is created through free of~~ the first metal layer, ~~exposing a portion of the die for receiving the bond wires.~~
4. (original) The semiconductor package substrate of claim 3, wherein the underlying metal layer comprises a signal layer.
5. (original) The semiconductor package substrate of claim 4, wherein the first metal layer comprises a ground plane.
6. (original) The semiconductor package substrate of claim 4, wherein the signal layer is sandwiched between a pair of the dielectric layers.

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7. (currently amended) The semiconductor package substrate of claim 1, wherein the ~~plurality of~~ metal layers comprise copper.
8. (currently amended) The semiconductor package substrate of claim ~~[[1]]~~ 6, wherein the ~~plurality of~~ dielectric layers comprise bismaleimide triazine (BT)
- 9-15. (canceled)
16. (currently amended) A packaged semiconductor device comprising:
an integrated circuit die; and
a package substrate, wherein the package substrate further comprises:
a plurality of metal layers, ~~wherein the metal layers are separated by a dielectric layer, the metal layers further comprising:~~
an *n* metal layer, to which the integrated circuit die is attached;
an *n-1* metal layer disposed on a side of the *n* metal layer opposing the
integrated circuit die, wherein the *n-1* metal layer is connected to
the die by a plurality of bond wires;
an *n-2* layer; and
an *n-3* layer.
17. (original) The device of claim 16, wherein the *n-1* layer comprises a plurality of signal traces.
18. (original) The device of claim 17, wherein a ground plane is disposed above the signal traces.
19. (original) The device of claim 18, wherein the signal traces are sandwiched between a pair of the dielectric layers.

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20. (original) The device of claim 19, wherein one of the pair of the dielectric layers is a substrate core layer.
21. (original) The device of claim 18, wherein the $n-2$ metal layer comprises a power plane.
22. (original) The device of claim 18, wherein the $n-3$ metal layer comprises a land layer.

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